A 2–18 GHz Low-Noise/High-Gain Amplifier Module

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Abstract—**Earlier predictions [1] that the two-tier matrix amplifier possesses excellent low-noise potential have been verified. Experimental modules whose topology is based on a computer-optimized design exhibit an average noise figure of $F = 3.5$ dB with an associated average gain of $G = 17.8$ dB across the 2–18 GHz frequency band. These state-of-the-art results were achieved with GaAs MESFET's whose minimum noise figure is $F = 2.2$ dB at 18 GHz and whose gate dimensions are 0.25×200 μm. The design considerations and the test results are discussed in detail.**

I. Introduction

APPLYING THE additive and the multiplicative amplification processes, as they are combined in the two-tier matrix amplifier, to low-noise operation has been shown to hold excellent potential [1]. The concept and the practical realization of the matrix amplifier in the form of a 2×4 rectangular array have been described in the literature [2]. During the study of the theoretical noise behavior of this new device it was discovered that the matrix amplifier offers a most desirable compromise between its broad-band maximum noise figure on one hand and its gain as well as *VSWR* performance on the other. Following this lead, an attempt was made to apply what was learned from the theoretical results discussed in [1] to the design of a 2–18 GHz low-noise amplifier module. In contrast to the development effort reported in [1], in which the design emphasis was put on gain and *VSWR* performance, in this paper it is shifted to optimum noise characteristics. This endeavor has resulted in the achievement of the lowest noise figure and the highest associated gain in a 2–18 GHz MESFET amplifier module reported to date.

II. Optimized Gain Versus Optimized Noise Figure Design

In this chapter we discuss the design of two matrix amplifier modules optimized for either noise or gain performance with additional, although lesser, emphasis on minimization of the circuits' reflection coefficients. The computations of all parameters are executed by means of an in-house computer program based on the formulas published in [1]. This program has the advantage of tracing the noise figure to the individual components which cause the noise and thereby gives valuable information on the dominating noise sources and their influence across the frequency band. The final optimization process, however, makes use of SUPER-COMPACT (version 1.91) [3], which became commercially available in 1987. SUPER-COMPACT's computed results for noise figure and gain are identical to those based on the formulas published in [1].

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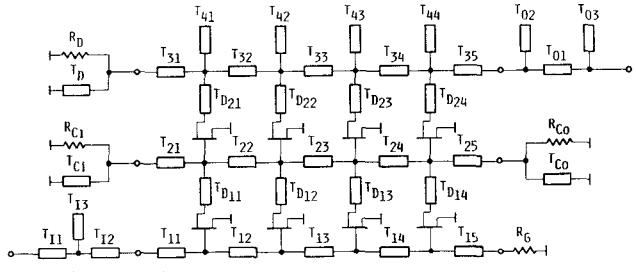

Fig. 1. Schematic of the two-tier matrix amplifier ($n = 4$).

A schematic of the two-tier matrix amplifier, incorporating $n = 4$ active six-ports, i.e., four identical transistors in each of the two tiers, is shown in Fig. 1. Each of the eight MESFET's, as well as each of the termination resistors R_G, R_{Ci}, R_{Co}, and R_D, injects noise power into the circuit that is reflected in the amplifier's noise figure [1]:

$$F = 1 + \frac{1}{G_s |Q_3|^2}\Bigg[|Q_1|^2 G_D + |Q_2|^2 G_{Ci} + |Q_4|^2 G_{Co} + |Q_5|^2 G_G + \sum_{k=1}^{n}\Big(|Q_6 - Y_{\text{cor}}^{(B)} Q_8|_k^2 R_{nk}^{(B)} + |Q_7 - Y_{\text{cor}}^{(A)} Q_9|_k^2 R_{nk}^{(A)} + |Q_8|_k^2 G_{nk}^{(B)} + |Q_9|_k^2 G_{nk}^{(A)}\Big)\Bigg]$$

where

- G_s source conductance,
- $(Y_{\text{cor}}^{(\,)})_k$ correlation admittance of the kth transistor in the first (A) or the second tier (B),
- $R_{nk}^{(\,)}$ noise resistance of the kth transistor in the first (A) or the second tier (B),
- $G_{nk}^{(\,)}$ noise conductance of the kth transistor in the first (A) or the second tier (B),
- Q_m transformation factors [1].

It should be pointed out here that each multiplication factor Q_m ($m = 1, 2, \ldots, 9$) not only is a function of all the line elements of the circuit, but also depends on all the

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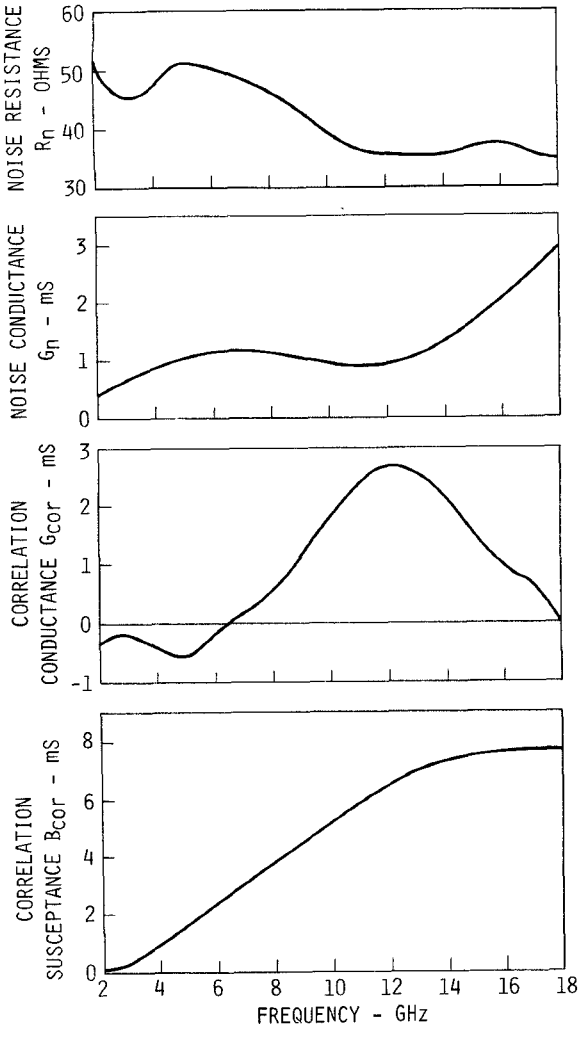

Fig. 2. The equivalent noise parameters of the GaAs MESFET.

terminations [1]. Due to the latter, we have $Q_m = f(Y_L, Y_D, Y_{Co}, Y_{Ci}, Y_G, Y_S)$, rendering the noise contributions of the individual termination conductances in (1) nonlinear functions of G_D, G_{Co}, G_{Ci}, G_G, and G_S.

The following computations are based on the noise parameters of a GaAs MESFET incorporating a 0.25 μm gate and processed on vapor phase epitaxial material. The data presented in Fig. 2 are computed from measurements of the minimum noise figure ($F_{\min}^{(DUT)}$), the noise measured when both the source and the load impedance are 50 Ω ($F_{50}^{(DUT)}$), and the optimum source admittance $Y_{S\min}$ at which $F_{\min}^{(DUT)}$ is obtained. The noise data based on these measurements and corrected for tuner losses are presented in Table I while a block diagram of the measurement system to determine the noise characteristics of the devices is shown in Fig. 3. It consists of a noise source, an input bias network, a slide-screw tuner as input admittance transformer, the device under test, an output admittance transformer, an output bias network, and a noise figure measurement system. The latter incorporates an isolator, a low-noise amplifier, a mixer, a local oscillator, and a noise figure meter. The 50 Ω input and output lines of the test fixture were characterized for their electrical lengths only

TABLE I
NOISE FIGURE DATA

FREQ Ghz	Fmin dB	Γopt Mag	Γopt Ang	F50 dB	Rn Ohm
2.0	1.00	0.75	0.5	3.05	51.7
3.0	1.20	0.69	1.5	2.85	45.7
4.0	1.35	0.65	6.0	2.90	47.0
5.0	1.50	0.63	10.0	3.10	52.3
6.0	1.65	0.62	14.5	3.10	48.7
7.0	1.75	0.61	18.5	3.15	48.4
8.0	1.80	0.61	22.5	3.15	46.4
9.0	1.85	0.61	27.0	3.15	44.2
10.0	1.95	0.60	31.0	3.10	39.4
11.0	2.00	0.60	36.0	3.10	37.0
12.0	2.05	0.59	39.0	3.10	35.7
13.0	2.05	0.58	42.0	3.10	35.8
14.0	2.10	0.56	44.0	3.10	35.5
15.0	2.10	0.54	46.0	3.10	36.7
16.0	2.15	0.51	47.0	3.10	37.7
17.0	2.15	0.48	48.0	3.00	36.1
18.0	2.15	0.44	50.0	2.90	35.2

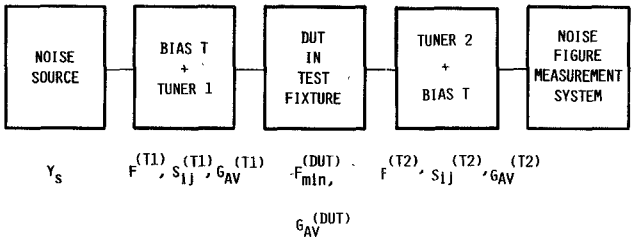

Fig. 3. Block diagram of the measurement system for the minimum noise figure.

and their losses were assumed negligible. For this idealized case, the test fixture has no influence on the minimum noise figure of the device under test $F_{\min}^{(DUT)}$. However, the measured optimum source admittance $Y_{S\min}$ requires a correction for the electrical length of the test fixture's input line. Additional information on the accurate measurement of minimum noise figures as they pertain to the losses of the tuner is given in the Appendix. The transistors' equivalent circuit and its element values as computed from the measured S parameters are shown in Fig. 4.

Table II compares the values of all circuit elements of the matrix amplifier when optimized for either gain or noise performance. The line dimensions are given for a 10-mil-thick substrate with a dielectric constant of $\epsilon_r = 3.78$. While the comparison reveals general trends such as equal or longer links of the low-noise design's gate and shorter links of its center lines when compared to the optimum gain module, the complicated nature of the dependency of the noise figure (1) on all circuit elements as well as the active devices makes it extremely difficult to formulate a set of general design rules. However, there are some simple guidelines that may be helpful in arriving at an optimum design. Throughout our theoretical and experimental studies we observed a high sensitivity of the noise figure to changes in the dimensions of the amplifier's circuit elements, especially over the upper portion of the frequency band. Due to this characteristic we arrived at the conclusion that when striving for the best noise figure,

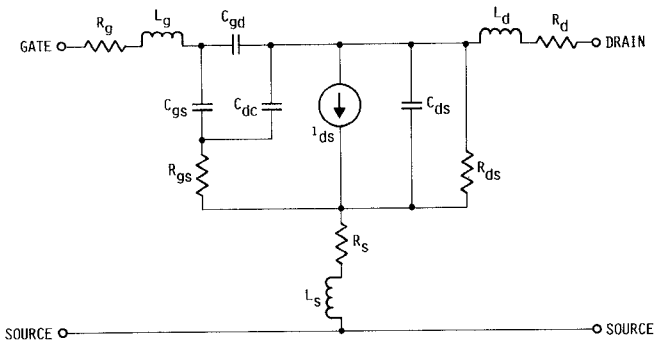

Fig. 4. Equivalent circuit and circuit elements of the GaAs MESFET.

Intrinsic Elements	*Extrinsic Elements*
$g_m = 30.0$ mS	$R_g = 6.4\ \Omega$
$\tau_0 = 1.2$ ps	$L_g = 0.149$ nH
$C_{gs} = 0.184$ pF	$R_s = 0.15\ \Omega$
$C_{gd} = 0.013$ pF	$L_s = 0.032$ nH
$C_{dc} = 0.047$ pF	$C_{ds} = 0.010$ pF
$R_{gs} = 3.3\ \Omega$	$R_d = 1.5\ \Omega$
$R_{ds} = 290\ \Omega$	$L_d = 0.538$ nH

TABLE II
CIRCUIT ELEMENTS OF THE OPTIMUM GAIN AND OPTIMUM NOISE FIGURE DESIGN

Element	Low Noise Design Width Mil	Length Mil	Resistance Ohm	High Gain Design Width Mil	Length Mil	Resistance Ohm
TI1	—	—	—	—	—	—
TI2	17.5	22	—	5.0	14	—
TI3	10.0	51	—	10.0	63	—
TO1	10.0	8	—	18.5	79	—
TO2	10.0	29	—	10.0	8	—
TO3	10.0	34	—	10.0	19	—
T11	2.0	12	—	2.0	12	—
T12	2.0	34	—	4.0	34	—
T13	2.0	57	—	2.0	35	—
T14	2.0	65	—	2.0	47	—
T15	2.0	100	—	2.0	35	—
T21	3.0	39	—	2.0	44	—
T22	3.0	45	—	2.0	50	—
T23	3.0	45	—	2.0	60	—
T24	3.0	45	—	2.0	54	—
T25	3.0	85	—	2.0	112	—
T31	3.5	143	—	2.0	174	—
T32	3.5	161	—	2.0	157	—
T33	3.5	186	—	2.0	159	—
T34	3.5	32	—	2.0	48	—
T35	10.0	37	—	26.5	23	—
RC1	—	—	22	—	—	23
TC1	1.5	205	—	1.5	301	—
RD	—	—	51	—	—	100
TD	1.5	325	—	1.5	205	—
RG	—	—	45	—	—	42
RCo	—	—	58	—	—	62
TCo	—	—	—	1.5	213	—
TD11	11.5	34	—	6.5	39	—
TD12	2.0	34	—	2.0	39	—
TD13	2.0	34	—	2.0	39	—
TD14	3.0	34	—	6.5	39	—
TD21	10.0	53	—	2.0	53	—
TD22	2.0	53	—	2.0	118	—
TD23	2.0	99	—	2.0	118	—
TD24	2.0	99	—	2.0	118	—
T41	—	—	—	—	—	—
T42	10.0	10	—	—	—	—
T43	10.0	54	—	10.0	47	—
T44	10.0	71	—	10.0	50	—

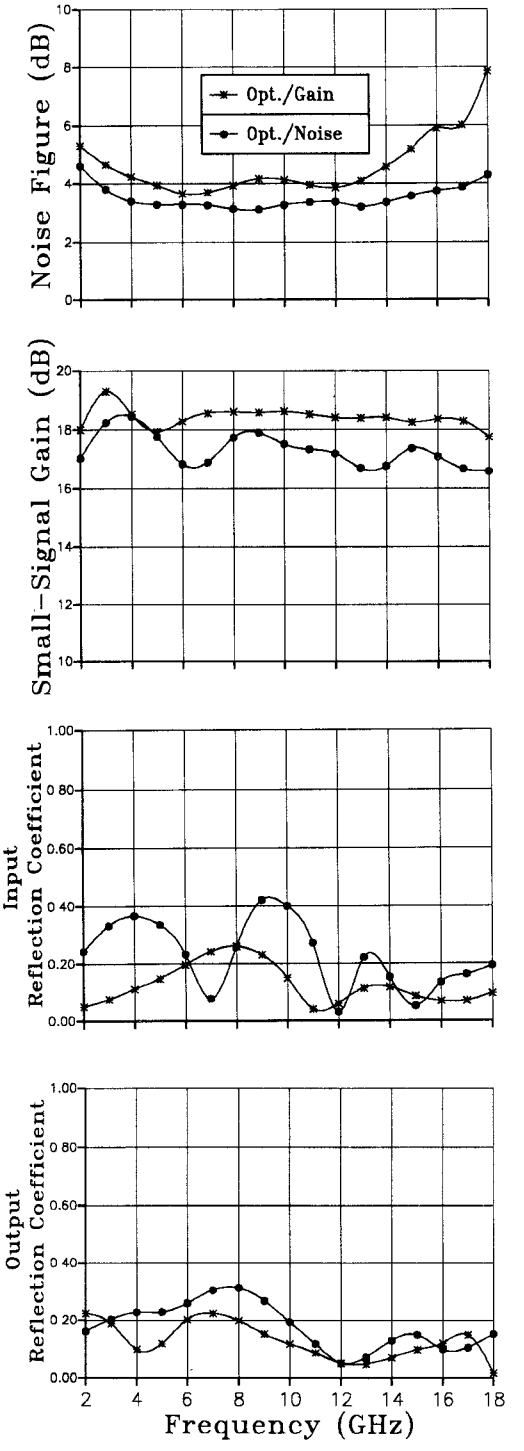

Fig. 5. Performance parameters of the matrix amplifiers optimized for either gain or noise figure.

it is advisable to start the computer design with all circuit elements individually subjected to the optimization process. Such a procedure, although time consuming, leads to the best possible performance. After the optimum design is known, the circuit may be gradually simplified due to concessions that are dictated by the layout or technological requirements. Each simplification may result in a degradation of the electrical performance and its implementation in the final design depends greatly on the design objectives, such as electrical performance, manufacturability, complexity, and cost.

The performance parameters of the two matrix amplifiers whose circuit elements were optimized for either gain or noise figure in accordance with the dimensions of Table II are shown in Fig. 5. The differences in noise figure range from a minimum of $\Delta F = 0.36$ dB to a maximum of $\Delta F = 3.88$ dB in favor of the optimized noise figure design. A look at the gain and reflection coefficients of both

TABLE III
PERFORMANCE DATA OF THE OPTIMUM GAIN AND THE OPTIMUM NOISE FIGURE DESIGN

SPECIFICATION \ DESIGN	OPTIMUM GAIN	OPTIMUM NOISE
GAIN - dB	18.98 ± 0.68	17.82 ± 1.07
MAX. NOISE FIGURE - dB	8.11	4.54
MAX. INPUT REFL. COEFF.	0.27	0.44
MAX. OUTPUT REFL. COEFF.	0.23	0.30

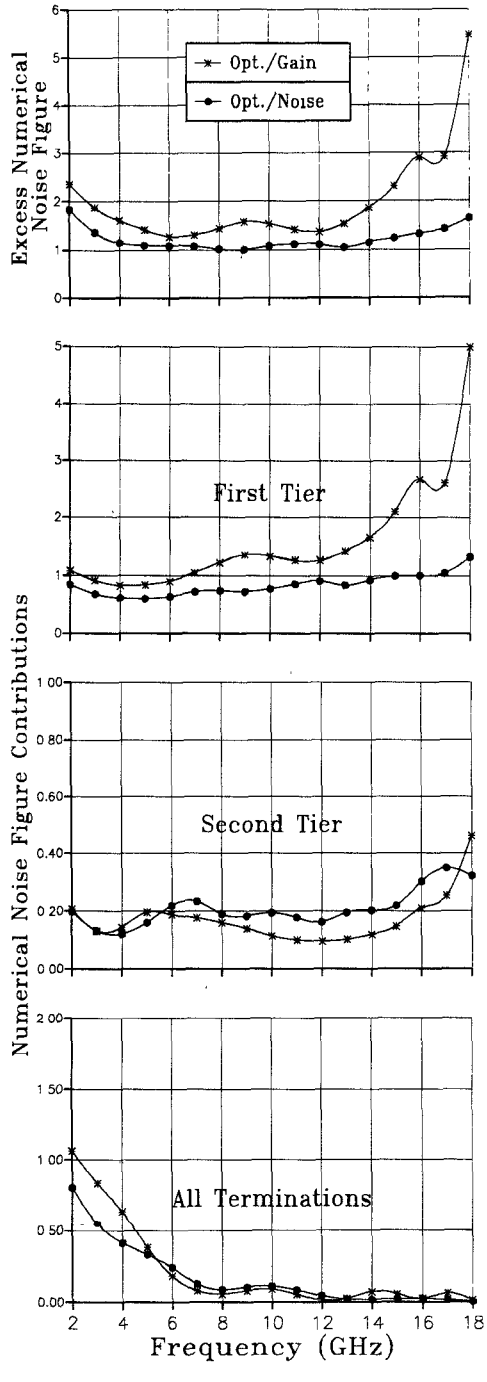

Fig. 6. Noise figure contributions of the matrix amplifiers optimized for either gain or noise figure.

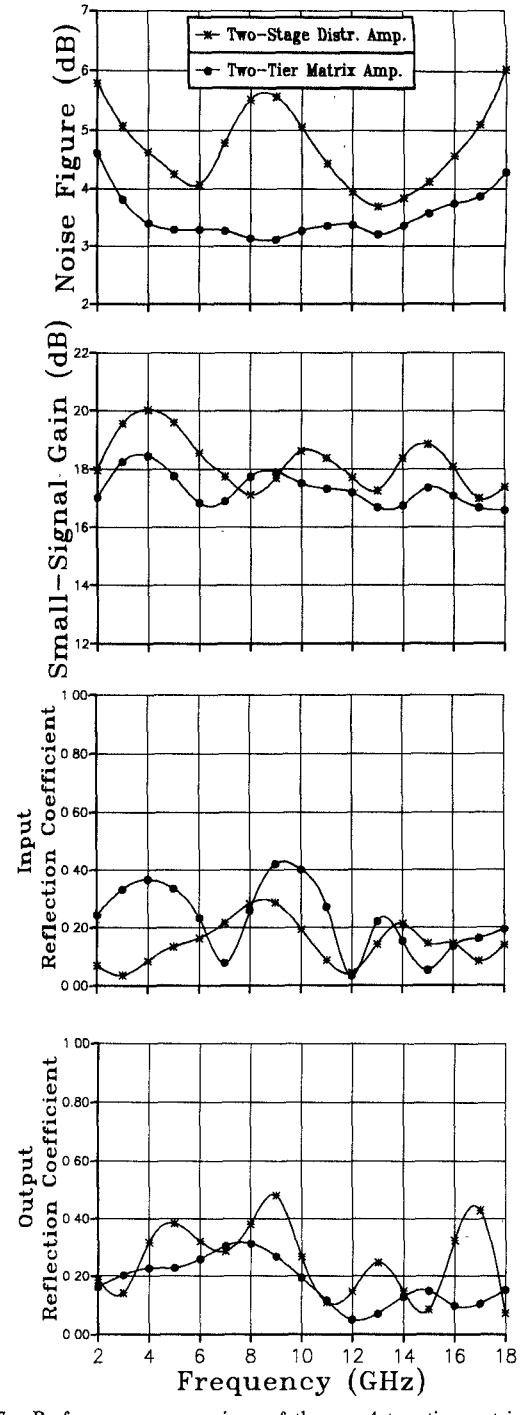

Fig. 7. Performance comparison of the $n = 4$ two-tier matrix amplifier with the equivalent two-stage distributed amplifier, both optimized for best noise performance.

amplifiers readily reveals the compromise that has been made. *VSWR*, gain, and gain variation have been traded for a significant improvement in the maximum noise figure. Table III summarizes the data represented in Fig. 5 and clearly demonstrates the trade-offs. The contributions of the first tier and the second tier of transistors, as well as those of all terminations to the overall excess numeric noise figure ($F-1$), are plotted in Fig. 6. Unquestionably, the first tier of devices contributes most of the noise. Note, however, how the optimum noise transformation keeps down the noise injected by the devices of the first tier,

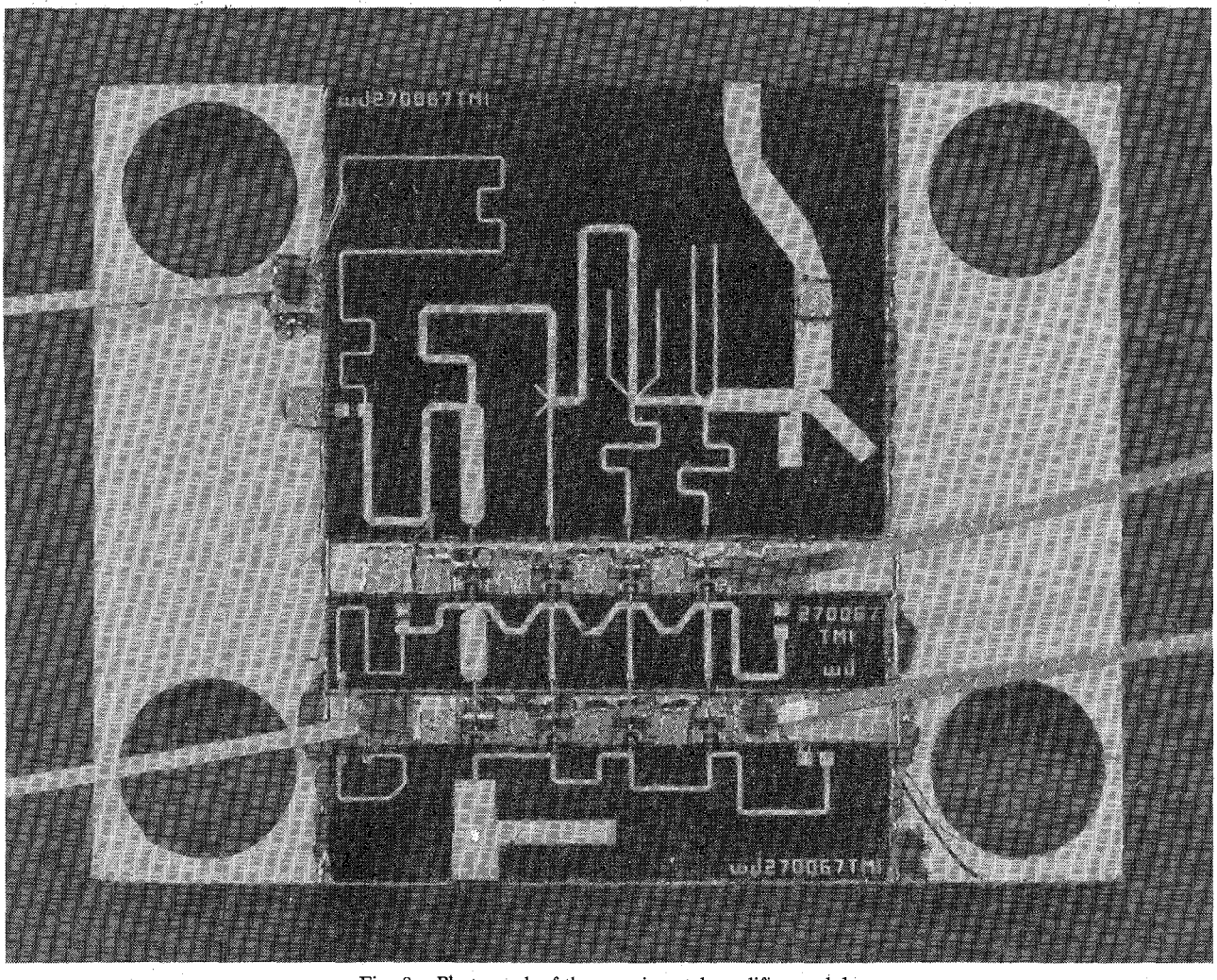

Fig. 8. Photograph of the experimental amplifier module.

especially at high frequencies. In contrast, the second tier's noise contribution of the optimum noise design exceeds that of the optimum gain design over most of the band. Finally, a closer examination of the noise originating in the terminations reveals that the lower contribution of the optimum noise design at the low-frequency end is mostly brought about by the transforming line elements rather than by the low-noise amplifier's slightly lower gate termination conductance G_G.

Before we focus our attention on the measured data of the experimental amplifiers, it seems appropriate to briefly compare the performance of the low-noise matrix amplifier with that of the equivalent two-stage distributed amplifier, when both are optimized for noise figure. In either device we employ eight identical GaAs MESFET's as they have been characterized earlier (Figs. 2 and 4). Both cascaded stages of the distributed amplifier are identical and are optimized as single-stage units. The differences in the performance characteristics of the matrix versus those of the two-stage distributed amplifier are reflected in Fig. 7. The comparison clearly shows the superiority of the matrix amplifier over the two-stage distributed amplifier when striving for the lowest noise operation. The maximum noise figures of the two devices differ by 1.4 dB while gain variations are ± 0.95 dB in the case of the matrix and ± 1.5 dB in the case of the two-stage distributed amplifier. Only the average gain and the input match of the distributed amplifier show better performance when compared with the matrix amplifier.

Based on the computations discussed in this chapter, we have found the matrix amplifier to be a device with excellent low-noise characteristics across multioctave frequency bands, offering an acceptable compromise between low-noise performance on one side and gain and *VSWR* performance on the other.

III. Experimental Performance of the Low-Noise Amplifiers

A. First Generation Design

The experimental low-noise amplifier module was laid out in accordance with the computed dimensions of Table II using 10-mil-thick fused silica as substrate material. A photograph of the module having an overall circuit size of 0.350×0.244 in. is shown in Fig. 8. A single voltage of 9.5 V was applied to a resistive divider network supplying the necessary voltages to the transistors. The MESFET's employed are those characterized by the data of Figs. 2 and 4.

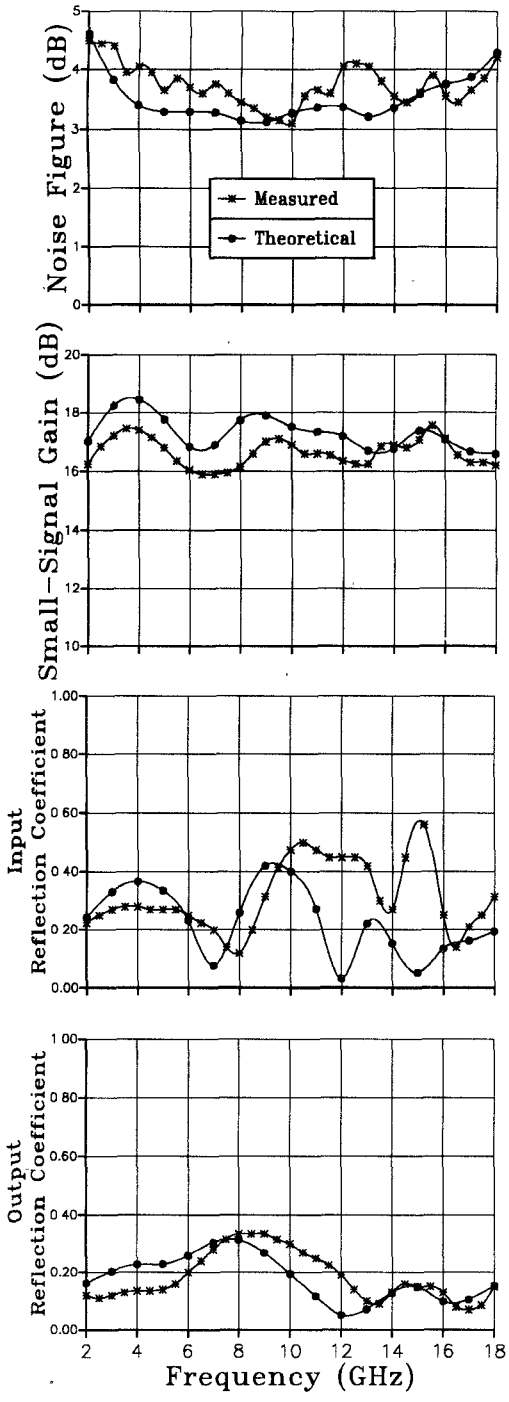

Fig. 9. Electrical performance of the first amplifier module (first generation).

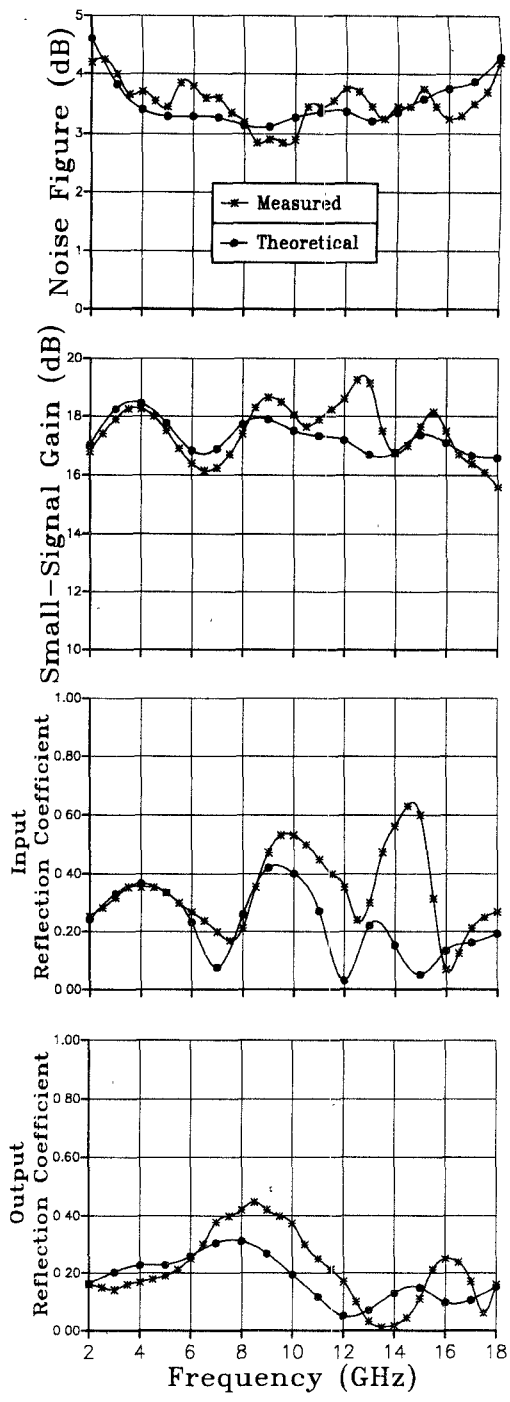

Fig. 10. Electrical performance of the second amplifier module after tuning for optimum noise figure (first generation).

The electrical performance of the first amplifier is reflected in the plots of Fig. 9, which also compares the measured and the computed data. The curves for noise figure, gain, and output reflection coefficient show excellent agreement between experiment and theory while those of the input reflection coefficient exhibit significant differences at high frequencies. The compromise that was made to obtain the optimum broad-band noise and gain performance shown in Fig. 9 is expressed in the relatively high input reflection coefficients. The latter reached a worst-case *VSWR* of 3.6:1. A maximum noise figure of $F = 4.5$ dB, an average noise figure of $F = 3.75$ dB, and a gain of $G = 16.7 \pm 0.8$ dB were measured across the 2–18 GHz frequency band. This performance corresponds to the single-stage maximum noise figure of approximately $F = 4.1$ dB that would be obtained if the gain were realized in a two-stage amplifier.

By making additional concessions to the input match and the gain variation we were able to further improve the noise figure. Optimizing for the noise figure by means of tuning some of the circuit elements on a second amplifier module yielded the data of Fig. 10, showing an improve-

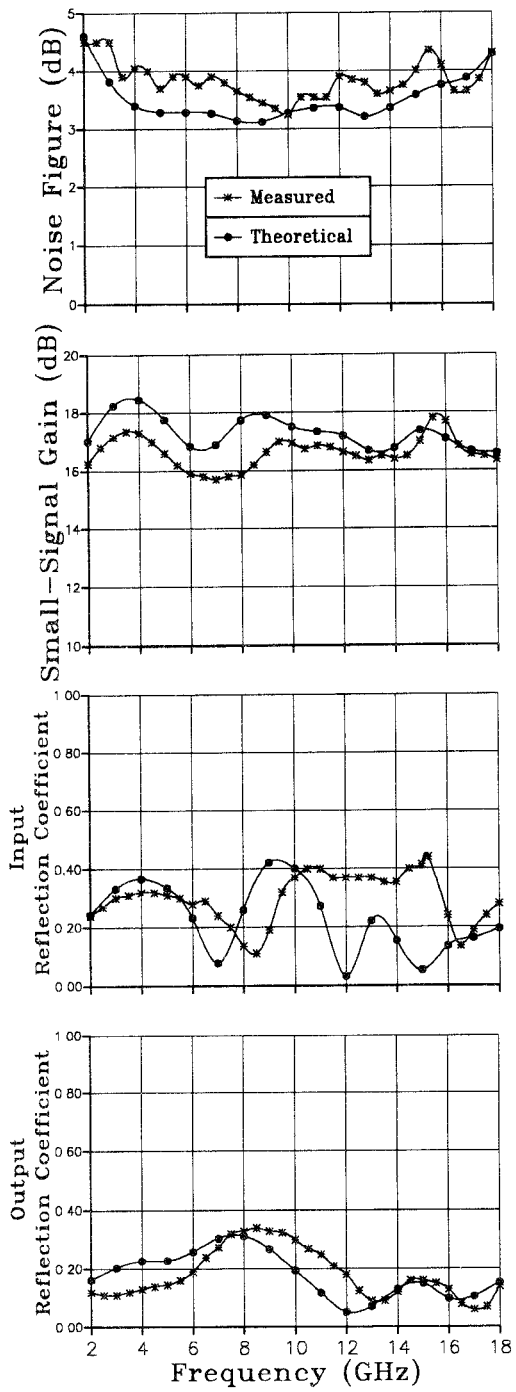

Fig. 11. Electrical performance of the first amplifier module after partial improvement of the input reflection loss.

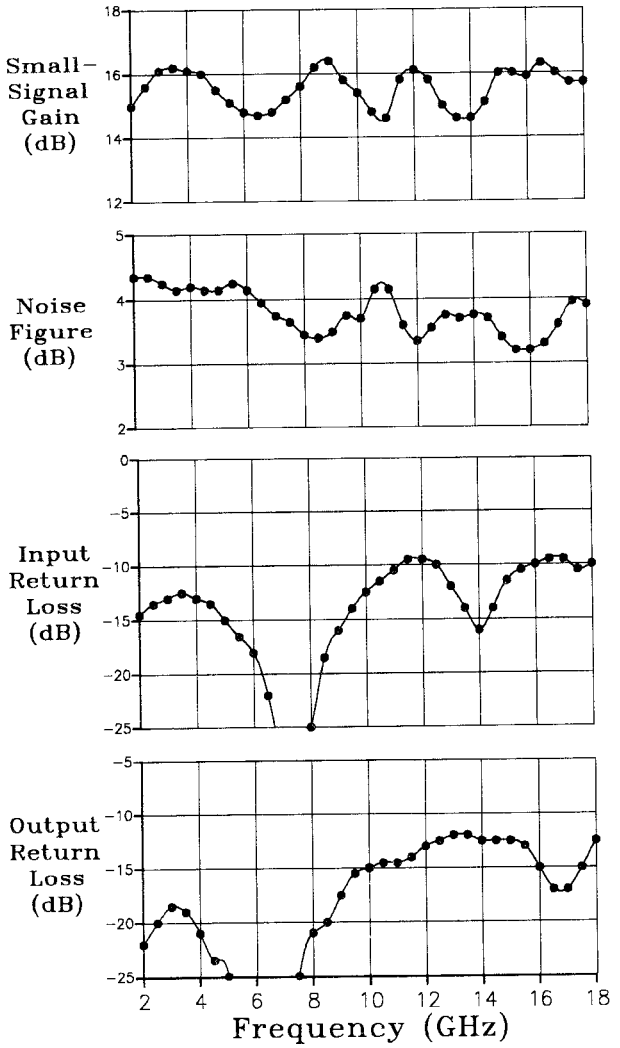

Fig. 12. Electrical performance of the second generation amplifier module.

ment of the maximum noise figure to $F = 4.25$ dB and of the average noise figure to $F = 3.53$ dB. However, in this module the gain variation deteriorated to $G = \pm 1.6$ dB and the maximum input *VSWR* increased to 4.4:1, with an average gain of $G = 17.8$ dB. Above results compare to a measured maximum noise figure of $F = 6.3$ dB, a gain of $G = 18.3 \pm 1.1$ dB, and a maximum input and output *VSWR* of 1.92:1 and 2.35:1, respectively [1], where the module was designed and tuned for best gain and *VSWR* performance but was operated over the narrower 2.5–18.0 GHz frequency band. The computed data plotted in Fig. 9 have been repeated in Figs. 10 and 11 for purposes of comparison.

Finally, an attempt was made to improve the input match of the first amplifier to a maximum return loss of $RL = -7$ dB without appreciably degrading the noise figure by adjusting the input circuit elements. The outcome of this effort is represented in Fig. 11. A comparison with the plots of Fig. 9 shows that both the maximum and the average noise figure did not degrade by more than 0.1 dB and were $NF = 4.6$ dB and $F = 3.84$ dB, respectively. However, the gain variation experienced a noticeable increase from $\Delta G = \pm 0.82$ dB to $\Delta G = \pm 1.15$ dB. In these experiments and those reported in [1], all MESFET's used in the amplifier modules were not only of the same type but were also taken from one and the same wafer.

As demonstrated in the experiments discussed so far and supported by the computer analysis, there is a trade-off between noise figure on the one hand and gain and input *VSWR* performance on the other. The specifications, as well as manufacturability and cost considerations, will dictate the compromises that have to be made to achieve the desired performance.

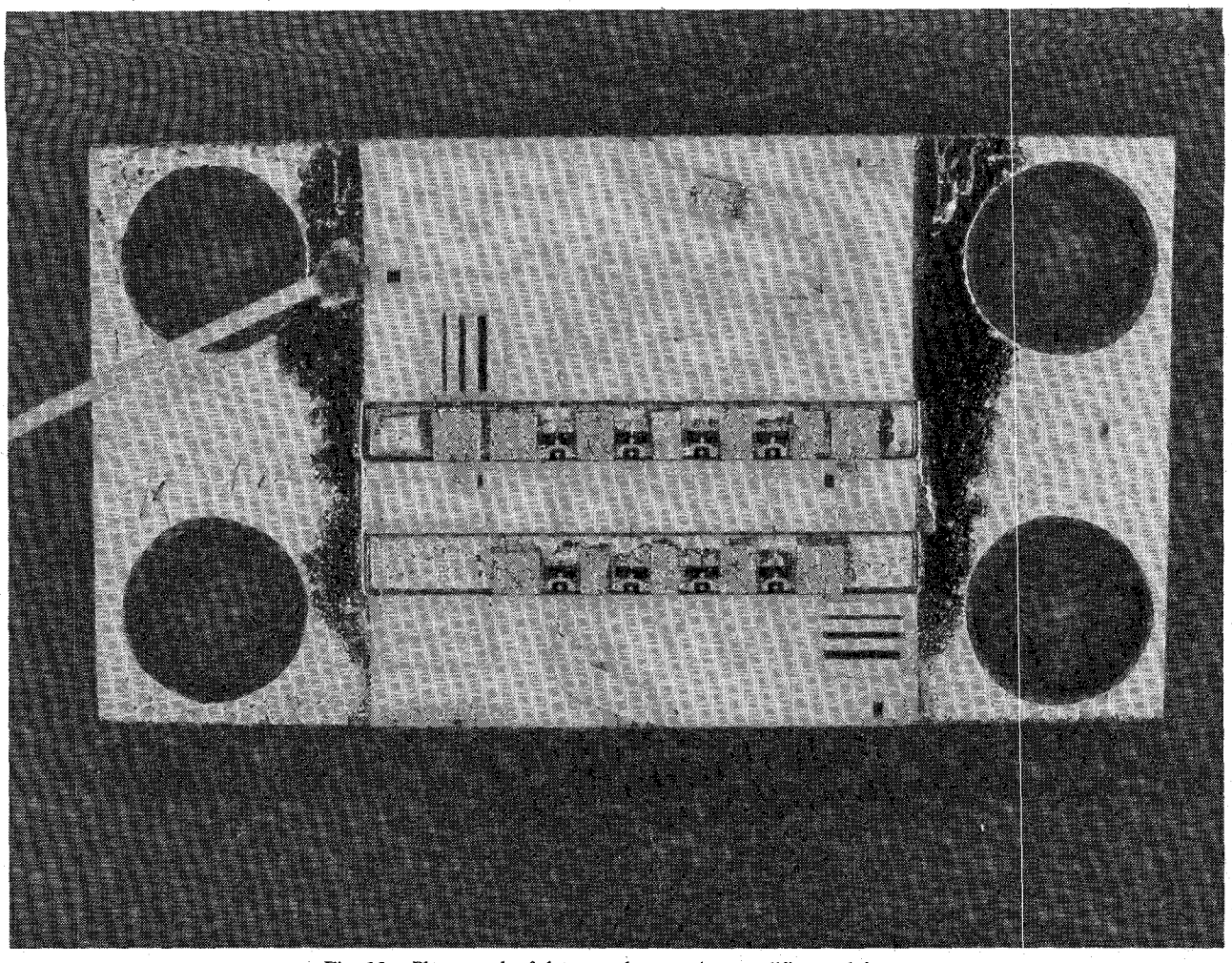

Fig. 13. Photograph of the second generation amplifier module.

B. Second Generation Design

In subsequent experiments we employed MESFET's that were fabricated with the same mask set on VPE material but with a somewhat shorter gate width. The resulting approximately 30 percent reduction in the gate–source capacitance (C_{gs}) when compared to the value given in Fig. 4 provided some improvement for the module's overall performance. Experimental results using this device in a second generation low-noise amplifier fabricated on 15-mil-thick alumina ($\epsilon_r = 9.8$) are displayed in the graphs of Fig. 12 while a photograph of this module is shown in Fig. 13. The unit is self-biased and operates at a single voltage of 8.5 V with a total current of 99 mA. As is readily discernible from Fig. 13, all biasing circuitry is deposited on the circuit substrates. The overall circuit dimensions of this unit are 0.230×0.250 in. At significantly improved input reflection coefficients when compared with the results discussed earlier of $|S_{11}| \leq 0.33$ (maximum return loss $= -9.5$ dB), noise figures of $F = 3.8 \pm 0.55$ dB and gains of $G = 15.4 \pm 0.8$ dB were recorded.

IV. Conclusions

The effectiveness of the two-tier matrix amplifier as a very low noise device with very high associated gains across multioctave frequency bands has been theoretically and experimentally demonstrated. Experimental modules of the first generation design whose topologies are based on a computer-derived design have yielded noise figures of $F = 3.5 \pm 0.7$ dB and $F = 3.8 \pm 0.7$ dB with associated gains of $G = 17.8 \pm 1.6$ dB and $G = 16.7 \pm 0.8$ dB, respectively. Likewise, noise figures of $F = 3.8 \pm 0.55$ dB and gains of $G = 15.4 \pm 0.8$ dB at associated reflection coefficients of less than 0.33 were measured on a second generation amplifier, fabricated on alumina and incorporating a current reducing biasing scheme. These results are believed to represent the lowest noise figures and highest associated gains across the 2–18 GHz frequency band reported to date. The achievement gains even more significance when considering the fact that the data were obtained with MESFET's that do not represent state-of-the-art low-noise devices. Beyond the experimental verification of the theoretically predicted performance characteristics, the paper compared the performance of a 2×4 matrix amplifier module that has been designed for optimum noise figure with one that has been designed for optimum gain characteristics. Noise figure differences as high as $\Delta F = 3.88$ dB occur at the high end of the band. In addition, a comparison between the optimum low-noise designs of a 2×4 matrix amplifier and its equivalent two-stage distributed amplifier was drawn.

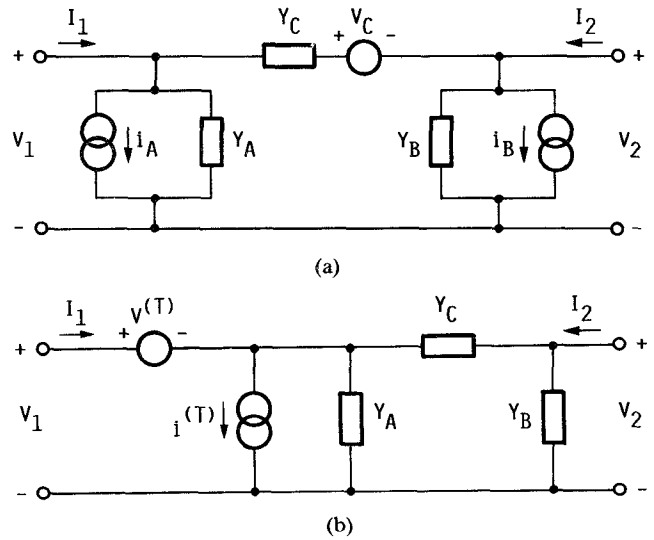

Fig. 14. Equivalent circuit of the lossy tuner, including its noise sources.

Appendix
The Admittance Transformer's Noise Characteristics

The accurate measurement of minimum noise figures is one of the more difficult tasks in the field of measurement techniques and corrections because of lossy tuning elements play a major role and thereby add to the uncertainties in the accuracy of the test results. Since the minimum noise figure represents one of the four quantities that fully characterize a noisy linear two-port, its value is an essential ingredient to the design of low-noise amplifiers.

In a recent paper [4], Cappy briefly reviewed the two widely used methods for accurately determining the device minimum noise figure. Both methods require changing or tuning the source admittance Y_S, which may be accomplished by means of a tuner. Unfortunately, such tuners have losses that generate thermal noise. Since there is some confusion about the tuner's quantitative role as a noisy two-port, it might be beneficial to briefly review this subject by determining the tuner's noise figure from its noise parameters.

The tuner or admittance transformer is a passive linear two-port that may be represented by the equivalent circuit of Fig. 14(a). It incorporates three thermal noise sources (i_A, i_B, and v_C) that fully characterize the noise properties of the device. The currents I_1 and I_2 of the circuit in Fig. 14(a), are given by

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} (Y_A + Y_C) & -Y_C \\ -Y_C & (Y_B + Y_C) \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} 1 & 0 & -Y_C \\ 0 & 1 & Y_C \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ v_C \end{bmatrix}. \tag{A1}$$

The relationship between the admittances in (A1) and the short-circuit admittance parameters of the tuner $Y_{ij}^{(T)}$ is described by

$$Y_A = Y_{11}^{(T)} + Y_{12}^{(T)} \tag{A1a}$$

$$Y_B = Y_{22}^{(T)} + Y_{12}^{(T)} \tag{A1b}$$

$$Y_C = -Y_{21}^{(T)} = -Y_{12}^{(T)}. \tag{A1c}$$

Using (A1), the transformation of the noise sources i_A, i_B, and v_C to the tuner's input in accordance with Fig. 14(b) results in

$$v^{(T)} = v_C + \frac{1}{Y_C} i_B \tag{A2a}$$

and

$$i^{(T)} = i_A + \frac{Y_A + Y_C}{Y_C} i_B + Y_A v_C \tag{A2b}$$

rendering the tuner itself noiseless. Taking into account that the noise sources of Fig. 14(a) are not correlated with each other, we find, for the characteristic noise parameters of the tuner,

$$R_n^{(T)} = \frac{\overline{|v^{(T)}|^2}}{4kT_0\Delta f} = \frac{(G_B + G_C)}{|Y_C|^2} \tag{A3a}$$

$$G_n^{(T)} = \frac{1}{4kT_0\Delta f}\left[\overline{|i^{(T)}|^2} - \frac{\overline{|i^{(T)}v^{(T)*}|^2}}{\overline{|v^{(T)}|^2}}\right] = G_A + \frac{G_B G_C}{(G_B + G_C)} \tag{A3b}$$

$$Y_{\mathrm{COR}}^{(T)} = \frac{\overline{i^{(T)}v^{(T)*}}}{\overline{|v^{(T)}|^2}} = Y_A + \frac{G_B}{(G_B + G_C)} Y_C \tag{A3c}$$

where

k Boltzmann's constant,
T_0 standard noise temperature (290 K),
Δf noise bandwidth.

The noise figure of a linear two-port, expressed by its characteristic noise parameters, is [5], [6]

$$F = 1 + \frac{1}{G_S}\left[G_n + R_n|Y_S + Y_{\mathrm{COR}}|^2\right]. \tag{A4}$$

Applying (A4) to the tuner, we obtain with (A3) the tuner's noise figure.

$$F^{(T)} = 1 + \frac{1}{G_S}\left[G_A + \frac{G_B G_C}{(G_B + G_C)} + \frac{G_B + G_C}{|Y_C|^2}\left|Y_S + Y_A + \frac{G_B}{G_B + G_C} Y_C\right|^2\right]. \tag{A5}$$

The available gain of the tuner shown in Fig. 14(a) for an arbitrary source admittance $Y_s = G_s + jB_s$ is given by

$$G_{\mathrm{AV}}^{(T)} = \frac{G_S}{G_2^{(T)}}\left|\frac{Y_C}{Y_A + Y_C + Y_S}\right|^2 \tag{A6a}$$

where

$$Y_2^{(T)} = G_2^{(T)} + jB_2^{(T)} = Y_B + Y_C - \frac{Y_C^2}{Y_A + Y_C + Y_S} \quad \text{(A6b)}$$

and

$$G_2^{(T)} = G_B + \frac{G_C|Y_A + Y_S|^2 + (G_A + G_S)|Y_C|^2}{|Y_A + Y_C + Y_S|^2}. \quad \text{(A6c)}$$

In the case where the source inductance is $Y_s = Y_0 = 20$ mS, the available gain of (A6a) can be easily expressed in terms of the tuner's S parameters, namely [4], [7]

$$G_{AV}^{(T)} = \frac{|S_{21}^{(T)}|^2}{1 - |S_{22}^{(T)}|^2}. \quad \text{(A7)}$$

By inserting (A6c) into (A6a) and comparing it with (A5), we obtain the important relationship between the available gain of the tuner $G_{AV}^{(T)}$ and its noise figure $F^{(T)}$ [7]

$$F^{(T)} G_{AV}^{(T)} = 1 \quad \text{(A8)}$$

for the case where the source admittance Y_s and the tuner are at the same temperature. Equation (A8) holds true for any linear passive two-port and states that the noise power available from the source is identical to that available from the tuner, regardless of the source admittance Y_s.

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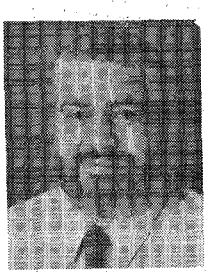

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